# Spatiotemporal Pattern Recognition with Neuromorphic Processor for Edge Applications*

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Deep Neural Networks (DNNs) are used to obtain state-of-art performance on a broad range of tasks. Most DNNs are implemented in von Neumann computing systems that are highly flexible and not ideally suited for such massively parallel architectures, which leads to energy-inefficient solutions that require more power than necessary by several orders of magnitude. A different approach is required to enable training and usage of DNNs in edge applications, such as wireless sensors for industrial condition monitoring, where high-frequency signals need to be processed over extended periods of time with a limited power supply.

Spiking Neural Networks (SNNs) implemented in neuromorphic processors is one possible approach. Such low-power computing systems approximate the dynamics of biological neurons with transistors operating in the sub-threshold regime, where the current-voltage dependence is governed by the same diffusion law as the charge transport in ion channels of neurons. Neuromorphic processors also offer possibilities to translate advances in neuroscience to cognitive computing architectures. However, further research and development of tools are required to make engineering applications of neuromorphic processors feasible.

This Ph.D. project focuses on developing methods and tools for spatiotemporal pattern recognition with SNNs implemented in the DYNAP family of neuromorphic processors. SNNs offer an interesting computational model for pattern recognition (**Fig. 1A**), which does not necessarily require iterations or feedback connections to process spatiotemporal patterns [1]. The DYNAP-SE (**Fig. 1B**) uses a combination of inhomogeneous analog circuits and programmable digital circuits for the emulation of SNNs with bio-physically realistic neuronal and synaptic behaviors [2], making it a low-power platform for spike-based neural processing with co-localized memory and computation.

Delays are essential computational elements for processing temporal spike patterns [6]. Temporal delays have, for example, been implemented in neuromorphic hardware by the use of dedicated, specifically tuned delay neurons [5]. In order to exploit the full computational capacity of SNNs and make efficient use of the hardware, however, we propose exploiting synaptic dynamics to allow large fan-in and pattern recognition by each neuron [1]. Inspired by the auditory system of crickets, which has a non-spiking delay mechanism based on post-inhibitory rebound [4], we have invented a synaptic delay element (**Fig. 1C**) for neuromorphic hardware that combines the dynamics of one inhibitory and one excitatory synapse [3]. These elements can be configured to generate excitation

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delays of the order of 10-100 ms. Our current work focuses on characterizing the dynamics of SNNs with such delay elements configured in the DYNAP-SE, and on spatiotemporal pattern recognition applications (**Fig. 1D**).

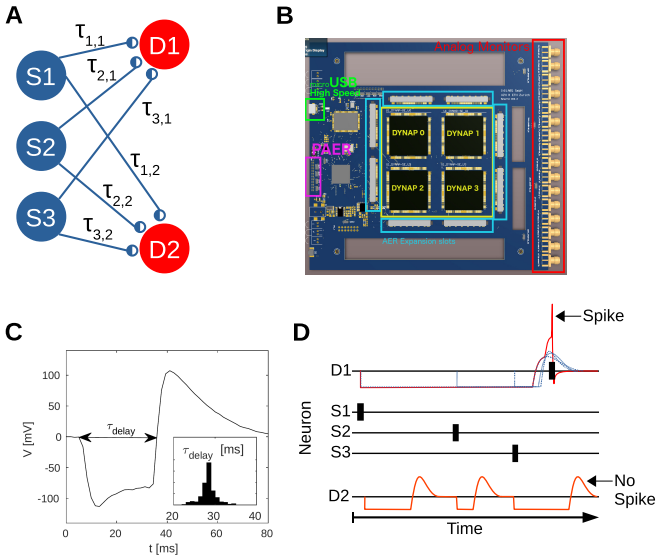


**Fig. 1. (A)** SNN for spatiotemporal pattern recognition with input neurons (S1-S3) and feature detectors (D1-D2). The half-filled disks denote synaptic delay elements that produce post-inhibitory delayed excitations. **(B)** DYNAP-SE neuromorphic system (`aictx.ai/technology`), comprising four four-core chips, each with 1k (64k) silicon neuron (synapse) circuits that dissipate 0.95 mW at 1.8 V and 30 Hz spike frequency. **(C)** Silicon neuron membrane potential for one presynaptic spike received by a delay element, and the distribution of delays for the 256 neurons in one DYNAP-SE core. **(D)** Example of spike pattern from S1-S3 detected by D1 but not by D2 at cost 5.3 pJ.

## References

1. Mauk, M.D., Buonomano, D.V.: The neural basis of temporal processing. Annual Review of Neuroscience **27**(1), 307–340 (2004)
2. Moradi, S., Qiao, N., Stefanini, F., Indiveri, G.: A scalable multicore architecture with heterogeneous memory structures for dynamic neuromorphic asynchronous processors (dynaps). IEEE Trans. Biomed. Circuits Syst. **12**(1), 106–122 (2018)
3. Nilsson, M.: Monte Carlo Optimization of Neuromorphic Cricket Auditory Feature Detection Circuits in the Dynap-SE Processor. Master's thesis, LTU (2018)
4. Schöneich, S., Kostarakos, K., Hedwig, B.: An auditory feature detection circuit for sound pattern recognition. Science Advances **1**(8), e1500325 (2015)
5. Sheik, S., Coath, M., Indiveri, G., Denham, S.L., Wennekers, T., Chicca, E.: Emergent auditory feature tuning in a real-time neuromorphic vlsi system. Frontiers in neuroscience **6**, 17 (2012)
6. Sheik, S., Pfeiffer, M., Stefanini, F., Indiveri, G.: Spatio-temporal spike pattern classification in neuromorphic systems. In: Conference on Biomimetic and Biohybrid Systems. pp. 262–273. Springer (2013)